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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
PEUGH, BRIAN R

ART UNIT	PAPER NUMBER
2187	8

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/641,519	RYAN, KEVIN J.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,13,14,17,18,22-29,35,36,39,40,45,46,49,50 and 54-58* is/are rejected.

7)☒ Claim(s) *8-12,15,16,19-21,30-34,37,38,41-43,47,48 and 51-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed April 28, 2003 in response to PTO Office Action dated January 27, 2003. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1 and 4-58 have been presented for examination in this application. In response to the last Office Action, claims 15, 37, and 47 have been amended.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 4-7, 13, 14, 17, 18, 22-29, 35, 36, 39, 40, 44-46, 49, 50, and 54-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Leung (US# 6,504,780).

Regarding claims 1 and 55, Leung teaches a system for hiding refresh operations in a dram device using clock division. Figures 4 and 6 diagram the signals used for the external access and refresh operations performed on the DRAM cells. By dividing the clock cycle into two portions, an external request can occur on a first portion of the clock cycle, while the refresh operation occurs on the second portion of the clock cycle (abs., lines 10-13; col. 15, lines 17-26). The description of figures 4 and 6, detailing the specific signals, is found in column 8, line 26 – column 10, line 10 and column 13, line 31 – column 14, line 53, respectively. For example, regarding figure 2 at time T2, both a read access and refresh access are found to be pending. The read access is applied at the start of time T2, while the refresh operation occurs in the latter half of cycle T2 (col. 11, line 62 – col. 12, line 3).

Regarding claims 4 and 5, since an external access and refresh operation can exist at the same time, but occur at different times within a cycle as detailed above, the access will occur first and not conflict with the refresh operation. The system of Leung operates in this way should the access and refresh operations correspond (conflict) with each other.

Regarding claims 6 and 7, and specifically regarding claim 6, the next available time slot as claimed would correspond to the refresh operation occurring in the latter half of the time slot (T2, for example). A second data access could appear during the refresh cycle and occur at the beginning of the next time cycle, since the claim does not

recite when the second data access occurs. Regarding claim 7, as can be seen form the timing diagram of figure 4, a second data access occurs just before the beginning of cycle T2 (WR# goes high, to indicate a write operation) during the refresh operation.

Regarding claims 13, 23, and 56, Leung teaches a system for hiding refresh operations in a dram device using clock division. Figures 4 and 6 diagram the signals used for the external access and refresh operations performed on the DRAM cells. By dividing the clock cycle into two portions, an external request can occur on a first portion of the clock cycle, while the refresh operation occurs on the second portion of the clock cycle (abs., lines 10-13; col. 15, lines 17-26). The description of figures 4 and 6, detailing the specific signals, is found in column 8, line 26 – column 10, line 10 and column 13, line 31 – column 14, line 53, respectively. For example, regarding figure 2 at time T2, both a read access and refresh access are found to be pending. The read access is applied at the start of time T2, while the refresh operation occurs in the latter half of cycle T2 (col. 11, line 62 – col. 12, line 3). The communication link as claimed could be any one of a number of signals as detailed in figure 4. For instance, the WR# signals is used for initiating a read or write operation. The controller as claimed refers to a memory array sequencer (122), which controls operations for the memory array (col. 5, lines 44-50), and a refresh controller (121) for controlling refreshing operations (co. 5, lines 6-7). As a result, external accesses can occur during a separate portion of the clock cycle than the refresh operation (col. 5, line 56 – col. 6, line 7).

Regarding claims 14 and 22, the WR# signal line, which carries a signal related to a read or write operation, would comprise a command/address bus as claimed.

Regarding claim 17, the refresh controller (as recited above) is part of the controller as claimed.

Regarding claim 18, counters (201) and (202) are incremented according to the CLK signal, where the CLK signal is used for all commands (col. 5, lines 19-32).

Regarding claim 24, the WR# signal line, which carries a signal related to a read of write operation, would indicate a read or write command at, for instance, the beginning of time cycle T2, as seen in Figure 6.

Regarding claim 25, the refresh operation occurs according to the refresh controller in the latter half of the time cycle (time slot), as recited above.

Regarding claims 26 and 27, since an external access and refresh operation can exist at the same time, but occur at different times within a cycle as detailed above, the access will occur first and not conflict with the refresh operation. The system of Leung operates in this way should the access and refresh operations correspond (conflict) with each other.

Regarding claims 28 and 29, and specifically regarding claim 6, the next available time slot as claimed would correspond to the refresh operation occurring in the latter half of the time slot (T2, for example). A second data access could appear during the refresh cycle and occur at the beginning of the next time cycle, since the claim does not recite when the second data access occurs. Regarding claim 7, as can be seen form the timing diagram of figure 4, a second data access occurs just before the

beginning of cycle T2 (WR# goes high, to indicate a write operation) during the refresh operation.

Regarding claims 35, 45, 57, and 58, Leung teaches a system for hiding refresh operations in a dram device using clock division. The invention relates to semiconductor memories using DRAM (col. 1, lines 31-33). Leung does not explicitly state incorporating a processor (claim 45) to control the DRAM memories, but one of ordinary skill in the art would recognize that a processor is inherently required for DRAM operations to occur. Figures 4 and 6 diagram the signals used for the external access and refresh operations performed on the DRAM cells. By dividing the clock cycle into two portions, an external request can occur on a first portion of the clock cycle, while the refresh operation occurs on the second portion of the clock cycle (abs., lines 10-13; col. 15, lines 17-26). The description of figures 4 and 6, detailing the specific signals, is found in column 8, line 26 – column 10, line 10 and column 13, line 31 – column 14, line 53, respectively. For example, regarding figure 2 at time T2, both a read access and refresh access are found to be pending. The read access is applied at the start of time T2, while the refresh operation occurs in the latter half of cycle T2 (col. 11, line 62 – col. 12, line 3). The communication link as claimed could be any one of a number of signals as detailed in figure 4. For instance, the WR# signals is used for initiating a read or write operation. The controller as claimed refers to a memory array sequencer (122), which controls operations for the memory array (col. 5, lines 44-50), and a refresh controller (121) for controlling refreshing operations (co. 5, lines 6-7). As a result,

external accesses can occur during a separate portion of the clock cycle than the refresh operation (col. 5, line 56 – col. 6, line 7).

Regarding claims 36, 44, and 54, the WR# signal line, which carries a signal related to a read of write operation, would comprise a command/address bus (communications link) as claimed.

Regarding claim 39, the refresh controller (as recited above) is part of the controller as claimed.

Regarding claim 40, counters (201) and (202) are incremented according to the CLK signal, where the CLK signal is used for all commands (col. 5, lines 19-32) for the DRAM memory.

Regarding claim 46, the WR# signal line, which carries a signal related to a read of write operation, would indicate a read or write command at, for instance, the beginning of time cycle T2, as seen in Figure 6.

Regarding claim 49, e refresh operation occurs according to the refresh controller in the latter half of the time cycle (time slot), as recited above.

Regarding claim 50 counters (201) and (202) are incremented according to the CLK signal, where the CLK signal is used for all commands (col. 5, lines 19-32) for the DRAM memory.

Allowable Subject Matter

Claims 8-12, 15, 16, 19-21, 30-34, 37, 38, 41-43, 47, 48, and 51-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed April 28, 2003 have been fully considered but they are not persuasive. Applicant argued that US Patent No. 6,415,353, of which the applied reference US Patent No. 6,504,780 is a continuation-in-part of, does not contain the subject matter upon which the current Office Action uses for support of the rejections. The '353 reference is a continuation-in-part of Leung et al., US Patent No. 5,999,474, which does contain support for the aforementioned rejections. For example, see Figure 4, col. 10, lines 60-66; col. 11, lines 3-6; col. 12, lines 11-12 & 27-29, col. 13, lines 34-45, regarding refresh cycle is delaying to occur after conflicting with an access request. The structure of the system is found in Figure 1, col. 4, line 45 – col. 5, line 11. Also, the refresh and timing systems are more broadly recite in col. 10, line 37 – col. 13, line 60.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

DS/BRP

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

June 13, 2003